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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,411	06/24/2005	Jeffrey A. Chapman	GB02 0251 US	9263
24738	7590	03/21/2006	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			AHMADI, MOHSEN	
		ART UNIT	PAPER NUMBER	
			2812	

DATE MAILED: 03/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/540,411	CHAPMAN, JEFFREY A.
	Examiner	Art Unit
	Mohsen Ahmadi	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on _____.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,2,4-6 and 9-13 is/are rejected.
- 7) Claim(s) 3,7 and 8 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 24 June 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 - Certified copies of the priority documents have been received in Application No. _____.
 - Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 06/24/05
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____.

DETAILED ACTION

The application number 10/540411 for a "Method of Fabricating a TFT Device Formed by Printing" filed Dec 24, 2002 has been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 11-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Seiichi (JP Pat. 60133758).

Regarding claim 1, Seiichi discloses a method of providing a layer structure, forming a first patterned layer onto a surface of layer structure so as to mask a first region of surface, forming a second patterned layer onto surface layer of layer structure so as to mask a second region of surface and to leave unmasked a third region of surface (where the regions are source, gate and drain), etching layer structure in third region and removing first patterned layer and etching layer structure in first region, wherein at least one of first or second patterned layers is formed by printing (See abstract).

Regarding claim 2, Seiichi discloses a method wherein the first and second patterned layers are formed by printing (See abstract).

Regarding claim 11, Seiichi discloses a method when printing of first layer includes defining regions for forming source and drain terminals (See abstract).

Regarding claims 12 and 13, Seiichi discloses, fabricating a thin-film transistor comprising: printing means, configured to print a first patterned layer on a layer structure and a second, different patterned layer on a layer structure, etching means, configured to layer structure and removing means, configured either to remove first patterned layer and to leave at least part of second patterned layer or to remove second patterned layer and to leave at least part of first patterned layer (See abstract).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Seiichi (JP Pat. 60133758) in view of Yoshiharu et al. (EP 0471 628).

Regarding claim 4, Seiichi discloses all of the claimed features as stated above except for printing second patterned layer occurs substantially immediately following the printing of the first layer.

Yoshiharu et al. discloses a method of making a thin film transistor circuit wherein the method includes at least one step of a printing process for preparing ink patterns to define the area to be affected by the application of an etching process.

Yoshiharu et al. discloses a method of printing second patterned layer occurs substantially immediately following the printing of the first layer (See col. 4 lines 5-58).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the printing second patterned layer substantially immediately following the printing of the first layer as discloses by Yoshiharu et al. in the process of Seiichi for it's known benefit of accessing source and drain contact wires.

Regarding claim 5, Seiichi discloses all of the claimed features as stated above except for printing first patterned layer having a first thickness and printing second patterned layer having a second, different thickness.

Yoshiharu et al. discloses a method wherein the printing of first patterned layer has a first thickness and printing second patterned layer having a second, different thickness (See col. 4 lines 45-58).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the different thickness of first and second pattern layers as disclosed by Yoshiharu et al. in the process of Seiichi for it's known benefit of forming gate insulation and gate electrodes.

Regarding claim 6, Seiichi discloses all of the claimed features as stated above except for using first ink to print first patterned layer and a second ink to print second patterned layer.

Yoshiharu et al. discloses a method wherein the first and second ink are used to print the first and second patterned layer (See cols. 4 and 6 lines 5-35 and 23-33).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to use the first and second ink for printing as disclosed by Yoshiharu et al. in the process of Seiichi for it's known benefit of filling grooves.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong (US Pat. 2002/0187592).

Regarding claims 9 and 10, Figure 2E, of Wong shows a method of providing a substrate 100, providing a patterned conductive gate region 102 on substrate 100, providing a dielectric layer (silicon oxide or silicon nitride) 104 overlying substrate 100 and patterned conductive gate region 102, providing a first semiconductor layer (amorphous silicon) 106 overlying dielectric layer 104, providing a second semiconductor layer 108 overlying first semiconductor layer 106 and providing a metallization layer 110 overlying second semiconductor layer 108 (See page. 2 paragraphs [0024-0032]).

Allowable Subject Matter

Claims 3, 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The cited prior art does not disclose or suggest the method wherein printing of second patterned layer comprises: overlapping second patterned layer with at least a portion of first patterned layer and wherein first and second inks are different and first and second inks are diluted to different concentrations.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsen Ahmadi whose telephone number is

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1-571-272-5062. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 1-571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MA MA
03/07/2006


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER